soopendays

5. - 7. December 2012

so logic

so-logic GmbH Co KG
DI Peter Thorwartl
Lustkandlgasse 52
A-1090 Vienna, Austria

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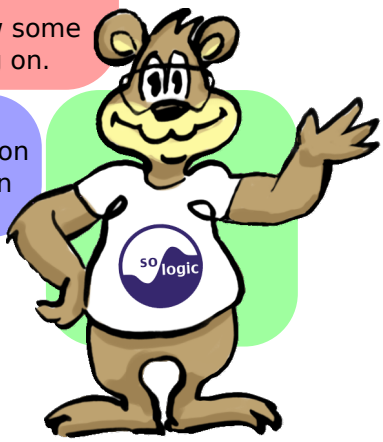
Introduction

We would like to present all new products and tools that Xilinx announced this year.
ZYNQ, the embedded processing platform, together with the new tools of VIVADO. The attendees should get a lot of new technical information, not only marketing material. Nowadays for a good FPGA design you need many different skills, we are happy to show with our partners everything to do a good design job. During and after the presentations we offer you a great platform to discuss your experiences and share your knowledge with other participants and partners.

We selected a historical place for this event and the participants can also make a tour through the building.
so-logic will offer also presentations and show some actual hardware from projects we are working on.

Lunch, dinner, beverages, coffee, tea and soft drinks will be included. Also an art exhibition will take place during the three days, which can be vistited by our guests.



Registration

To register please visit so-logic.net click on the "Customers"-tab and login with your customer account. If you do not already have an account, you can create one on this page as well. Click on "Participations". Write in the order number: "soopendays2012_day1" for the first day, "soopendays2012_day2" for the second day, "soopendays2012_day3" for the third day.
For further information please contact us.

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Attendees are members of hight-tech companies, universities and research centers from Middle Europe and Near- and Middle-East. We expect between 50 and 100 participants each day. Last time we had 250 attendees in three days. We will invite people from countries where we do training and development work:

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Partners

Xilinx is the world’s leading provider of All Programmable FPGA's, SoC's and 3D ICs. These industry leading devices are coupled with a next-generation design environment and IP to serve a broad range of customer needs, from programmable logic to programmable systems integration.

During the whole event we offer an exhibition from our partners and so-logic

Analog Devices Inc. defines innovation and excellence in signal processing. ADI's analog, mixed-signal, and digital signal processing (DSP) integrated circuits (IC) play a fundamental role in converting, conditioning, and processing real-world phenomena such as light, sound, temperature, motion, and pressure into electrical signals to be used in a wide array of electronic equipment. But that doesn’t begin to capture the essence of what Analog Devices does for our customers, and ultimately for the end user.

SILICA, a division of Avnet Electronics Marketing EMEA, provides a comprehensive range of products from 24 semiconductor manufacturers along with design support and the full set of logistical and value added services to industrial and commercial customers throughout Europe.

"We are your competent and reliable partner. We offer customized and complete solutions. Our services comprise the assembly of high-value and complex mechatronic subassemblies and of complete devices and the development and manufacturing of electronic assemblies. When doing such, we place the highest priority upon achieving the greatest possible precision and quality." - **LENZING**

X.Test is the international designated reseller for Agilent Technologies. X.Test was founded in Apr 2010 by H TEST, Christian Bauer and Jakob Udier who have worked for Agilent over more than 10 years as technical sales. X.Test offers the broad Agilent portfolio from handheld DMMs, over oscilloscopes up to spectrum- and network analyzers. To bring more valuable solutions to its customers, X.Test is now also the official represantative in Austria for Flir R&D thermographic cameras and Haefely ESD test&measurement.

Our Company

Our business is centered in the fields of electronic consulting, development and training for technical applications as far as electrical engineering is concerned.
so-logic offers flexible ways to save your time - from simple code review to turn-key solutions. Highly specialized teams work to implement your concepts.

"As CEO of an innovative technical enterprise based in Vienna I am particularly proud of the great satisfaction and confidence regarding our international business partners. Their positive resonance confirms our claim to high-quality workmanship and forms the basis for high motivation of our entire team."
-Peter Thorwartl

Experience began in the early days of FPGA development
Beginning with the first commercially available FPGA families the so-logic team developed scientific and industrial solutions based on programmable logic. The ever-increasing capabilities of todays FPGAs and embedded controllers create new challenges in the design process.

so-logic has used these and other methods for customer projects:
embedded system development, hardware description languages, programming languages, operating systems, development tools, architectures of FPGAs and microprocessors, circuit design and layout, peripheral components, DSP techniques, system level design, open source development, network enabled services, ...

Let us help you to create your leading edge products of tomorrow!

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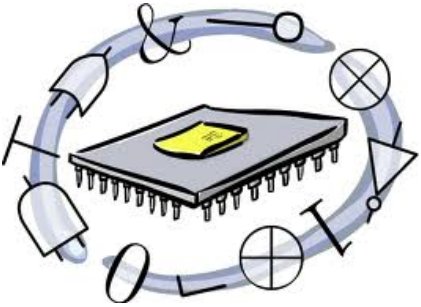
Schedule

1. Day

VIVADO™

7 series with Vivado



5. December 2012

Registration	10:00 - 11:00	**Track A**	**Track B**
Session1	11:00 - 12:15	Vivado Overview	High-Level Synthesis
Snacks	12:15 - 13:00		
Session2	13:00 - 14:30	Vivado Flow Overview	Analog Devices Connectivity
Session3	14:30 - 15:45	Simulation, IP Packager, Floorplanning	7 Series Overview
Break	15:45 - 16:15		
Session4	16:15 - 17:30	Constraints Flow and Tcl Scripting	Motor Control with Xilinx
Dinner	17:30 - 19:00		
Networking	19:00 - open end		

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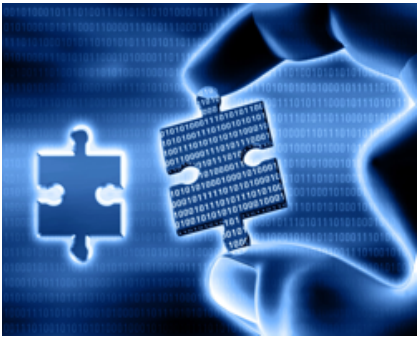
Schedule

2. Day



System Design with Vivado

6. December 2012

Registration	10:00 - 11:00	**Track A**	**Track B**
Session1	11:00 - 12:15	Embedded Processing	Vivado Overview
Snacks	12:15 - 13:00		
Session2	13:00 - 14:00	Wireless Communication with focus on SDR	Checking Signal Integrity of MultiGigabit-Transceiver
Session3	14:00 - 15:00	Sampling & Processing Real-World Data	IP Core Design
Break	15:00 - 15:30		
Session4	15:30 - 16:30	High-Speed Serial Communication	FPGA System Integration & IBIS-AMI Modeling
Session5	16:30 - 17:30	Designing for Signal & Power Integrity	High Level Manufacturing of Electronic Boards
Dinner	17:30 - 19:00		
Networking	19:00 - open end		

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Schedule

3. Day

Embedded Processing with ZYNQ

7. December 2012

Registration	10:00 - 11:00	**Track A**	**Track B**
Session1	11:00 - 12:15	Embedded Processing	Vivado Overview
Snacks	12:15 - 13:00		
Session2	13:00 - 14:00	Exploring Zed Board	FPGA Tutorial Courses & FPGA Database
Session3	14:00 - 15:00	Xilinx Strategic Directions	Designing for Signal & Power Integrity
Break	15:00 - 15:30		
Session4	15:30 - 16:30	Xilinx Industrial & Medical Imaging Solutions	Software Development
Session5	16:30 - 17:30	High-Level Synthesis	Open Source Linux Courses
Dinner	17:30 - 19:00		
Networking	19:00 - open end		

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Course Descriptions

7-Series Overview

Instructor: Wolfgang Mödinger, Xilinx **5.Dec 3B 14:30-15:45**

Built on the state-of-the-art 28nm HPL process technology, the 7 Series All Programmable FPGA family delivers breakout performance, capacity, and system integration while optimizing price/performance/watt.

Analog Devices Connectivity to Xilinx FPGAs

Instructor: Alex Tofan, Analog Devices **5.Dec 2B 13:00-14:30**

Checking the Signal Integrity of Multi-Gigabit-Transceiver

6.Dec 2B 13:00-14:00

Instructor: Dr. Thomas Kirchner, Agilent Technologies

When Multi-Gigabit signals are fed through long lines on PCBs, the reduced open eye caused by limited bandwidth and intersymbol interference can be compensated through ‚De-emphasis', equalization and distortion correction. The ‚Equalization Wizard' and comprehensive clock recovery methods allow the evaluation at a virtual point behind the equalizer and clock recovery. We will discuss DFE and FFE equalization methods, and we will answer the question of the optimum settings. We present real-time oscilloscopes with bandwidths up to 32GHz, which allow for a fast and simple test also on complex protocols and furthermore consists of a large amount of methods for failure evaluation and validation, like integrated serial trigger, protocol decoding, jitter- and eye diagram analysis, de-embedding of test fixtures and cabels/connectors.

Constraints Flow and Tcl Scripting

Instructor: Peter Thorwartl, so-logic **5.Dec 4A 16:15-17:30**

Talk about SDC, XDC, Vivado Tcl, Constraint Sets and how constraints can be applied/updated at each step of the flow. Then you will hear about XDC Constraints in IPs and the key difference between XDC and UCF and their Advantages. How to create basic Timing Constraints using GUI: Clocks, In, Outs. How to use Vivado tools (check_timing, report_clock_networks, etc.) to explore the design and correctly constrain it.

Designing for Signal and Power Integrity in FPGA Designs

6.Dec 5A 16:30-17:30

Instructor: Bernhard Greissing, so-logic **7.Dec 3B 14:00-15:00**

A short Overview of topics in Signal- and Power Integrity Issues that need to be addressed in High-Speed FPGA Printed Circuit Board Design. Issues to be tackled, rules of thumb, and pointers to additional resources.

Embedded System with the Zynq-7000 Extensible Processing Platform Devices

6.Dec 1A 11:00-12:00
7.Dec 1A 11:00-12:00

Instructor: Leopold Matzinger, so-logic

What is the Zynq-7000 EPP?
-Comparison of the processing system with other Xilinx Processing Solutions.
-Differences between programmable logic of Zynq and other Xilinx FPGAs.
-How to debug and simulate embedded systems with EPPs.

Exploring Zed Board

Instructor: Gerhard Nedok, Avnet **7.Dec 2A 13:00-14:00**

This course will give you an overview of the ZED board and the possibilities you have to get your Zynq design up and running faster.

FPGA System Integration and IBIS-AMI Modeling in SystemVue

Instructor: Ingo Nickeleit, X.Test **6.Dec 4B 15:30-16:30**

Today's communication systems involve complex DSP, which has to incorporateanalog/RF modeling in wireless and high serial interface applications. FPGAs enable a quick path to prototyping and flexible re-configuration. Despite ISE already offers a comprehensive selection of according DSP cores, increasing complexity imposes exploration and verification of DSP algorithms and architectures in overall system context, avoiding exhaustive implementation re-spins and on-chip debugging. This session will introduce an integrated design process validating interoperability of DSP and analog/RF using Agilent EEsof's SystemVue platform. With special respect to high speed SERDES interfaces we demonstrate the process of IBIS-AMI model generation and its reuse for on-board signal integrity simulations.

FPGA Tutorial Courses and FPGA Database

Instructor: Rastislav Struharik, so-logic **7.Dec 2B 13:00-14:00**

This presentation will introduce two free services offered by So-Logic: FPGA Tutorial courses, aimed primarily to the newcomers in the FPGA world; and the FPGA Database, a web-based database of all FPGA devices that have ever existed with a short demonstration.

High Level Manufacturing of Electronic Boards by Lenzing Technik Mechatronics

6.Dec 5B 16:30-17:30

Instructors: Roland Gammer and Norbert Leitner, Lenzing

After a general introduction to Lenzing Technik GmbH Mechatronics the presenters will talk about fully automated assembly of electronic boards:
- Components in SMT manufacturing
- The optimum soldering process
- Automated optical inspection
- Testing

High-Level Synthesis

5.Dec 1B 11:00-12:00

Instructor: Rastislav Struharik, so-logic **7.Dec 5A 16:30-17:30**

This presentation will introduce the key concepts of High-Level Synthesis and also what it brings to the contemporary FPGA design flow. During the presentation, Xilinx's new HLS tool, Vivado HLS, will be introduced and demonstrated.

High-Speed Serial Communication

Instructor: Peter Thorwartl, so-logic **6.Dec 4A 15:30-16:30**

Overview of different available Multi-Gigabit Transceivers and Protocols for Xilinx FPGAs, IP Cores, Wizards and Use Cases

IP Core Design and So-Logic's IP Cores

Instructor: Rastislav Struharik, so-logic **6.Dec 3B 14:00-15:00**

This presentation is about the concept of IP core development and usage, their importance in the current FPGA design methodology, as well as about the existing and future IP cores that are offered by So-Logic.

Motor Control with Xilinx

Instructor: Andreas Wolf, Silica **5.Dec 4B 16:15-17:30**

This course will show the challenges in today's motor control applications. It will show the new Spartan6 Motor Control Kit as well the benefits of Xilinx 7 Series for Motor Control.

Open Source Linux Courses for Xilinx FPGAs

Instructor: Herbert Groll, so-logic **7.Dec 5B 16:30-17:30**

TThis presentationwill show and demonstrate steps necessary to boot Linux on a microprocessor-based (MicroBlaze, PowerPC or ARM) embedded system built using some of all available Xilinx FPGA devices.

Sampling & Processing Real-World Data with FPGAs

Instructor: Gerhard Nedok, Avnet **6.Dec 3A 14:00-15:00**

This course will explore both the new XADC analog to digital converter component in the 7 series FPGAs as well as low and medium speed discrete ADCs and DACs, showing applications and techniques for boosting system performance.

Simulation, Floorplanning, IP Packager

Instructor: Peter Thorwartl, so-logic **5.Dec 3A 14:30-15:45**

-*Simulation*: Mixed Language simulation, Simulation sets, Simulation launch options, Memory Editor Analog Waveform Capability, Virtual Busses, Possibility to open Static Simulation

-*IP Packager:* Benefits of the IP Packager, IP Packager Flow, Create IP with some parameters (generics), Define version, compatibility, GUI, etc. Bundling with documentation, Packaging and importing into IP Catalog

-*Floorplanning*: Creation, resizing of Pblocks, Automatic Pblock Placement

Software Development

Instructor: Leopold Matzinger, so-logic **7.Dec 4B 15:30-16:30**

This course introduces you to software design and development for the Xilinx Zynq All Programmable System on a Chip (SoC) using the Xilinx Software Development Kit (SDK). You will learn the concepts, tools, and techniques required for the software phase of the design cycle.

Vivado Flow Overview

Instructor: Peter Thorwartl, so-logic **5.Dec 2A 13:00-14:30**

This course provides the overall context and framework for the development cycle of FPGAs. This course will give you an overview of proper planning techniques, strategy, and FPGA tool flow to get up and designing an FPGA design.

Vivado Overview

5.Dec 1A 11:00-12:15

Instructors: Wolfgang Mödinger, Xilinx **6.Dec 1B 11:00-12:15**

and Peter Thorwartl, so-logic **7.Dec 1B 11:00-12:15**

The Xilinx Vivado Design Suite is a revolutionary IP and system-centric design environment built from the ground up to accelerate the design of not only programmable logic in FPGAs but the design of 'All Programmable' SoCs and 3D ICs.

Wireless Communication with focus on SDR

Instructor: Alex Tofan, Analog Devices **6.Dec 2A 13:00-14:00**

Xilinx Industrial & Medical Imaging Solutions Overview

Instructor: Christian Stenzl, Xilinx **7.Dec 4A 15:30-16:30**

Xilinx FPGAs offer solutions for Motor Control, Industrial Networking, Industrial Imaging, Functional Safety and Medical Imaging applications through real-time performance with hardware-based soft IP, flexibility, in-system re-programmability with scalability across a common platform, particularly in the embedded space with the new Zynq-7000 All Programmable SoC Embedded Platform combining Dual-Cortex-A9 and flexible programmable logic.

Xilinx Strategic Directions

Instructor: Jens Schmidt, Xilinx **7.Dec 3A 14:00-15:00**

This presentor will talk about: 7 Series and Zynq Rollout, Next Generation Products, Markt Specific IPs and Vivado Software Packages

SO-Projects

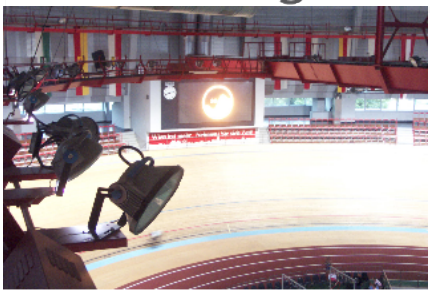
OrbiSat

OrbiSat
Radar System &
Remote Sensing

SCHIEBEL

SCHIEBEL Flight control for an Unmanned Aerial Vehicle (UAV)

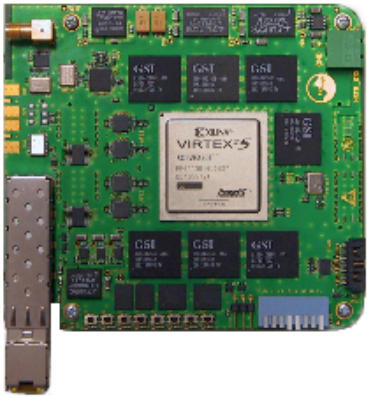
LED Voglhuber



Video Wall for the Ferry-Dusika-Stadium in Vienna together with Voglhuber

LANTIQ

LANTIQ HSFB-Board for ASIC Production Test



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Here is a short overview of some actual and previous projects of so-logic

RIEDEL
The Communications People

RIEDEL MediorNet Real-Time Network for Video, Audio, Data & Communications

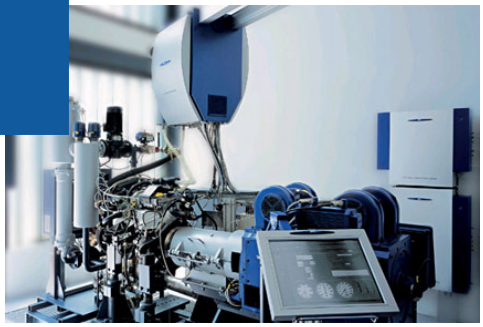
ARRI

ARRI Motion Contol System for cameras

durst

DURST Large Inkjet Printer

AVL



AVL Measurment Devices

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Location

WUK

Werkstätten- und Kulturhaus

Währinger Straße 59
A-1090 Vienna
www.wuk.at

History of WUK
Very close to our company, to Volksoper and also to the inner city of Vienna, surrounded by many hotels, restaurants and pubs the WUK has initially been built in 1855 as a locomotive factory. From 1884 to 1980 it has been home to the “Technological Trades Museum” (TGM), an institutional connection between research, exhibitions and training for technical professionals.

In 1979/1980 the building was abandoned and in a state of decay. In addition to several commercial and municipal plans there was always a strong interest in an “alternative” function. In the sociopolitical context of the evicted Arena, the spectacular youth protests in neighboring countries, alternative work and culture theoreticians and zero growth in the economy, social workers, artists, teachers, architects, feminist groups, students and pensioners came together united through the motto “Save the TGM” to discuss the content and material requirements for the creation of an alternative, autonomous cultural enterprise.

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Recommended Hotels

Here are our recommended hotels close to the event location. In these hotels you will also receive a discount from the regular price by announcing that you are there in connection to so-logic.

Hotel am Schottenpoint
Währinger Straße 22
A 1090 Vienna
+43 (1) 310 87 87 -0
hotel-schottenpoint.at

Hotel Alexander
Augasse 15
A-1090 Vienna
+43-1-317 15 08
hotel@alexander.co.at
www.alexander.co.at

Hotel Arkadenhof
Viriotgasse 15
A-1090 Vienna
+43-1-310-08-37-0
office@arkadenhof.com
www.arkadenhof.com

Hotel Bellevue
Althanstraße 5
A-1091 Vienna
+43-1-313-802
bellevue@austria-hotels.at
austria-hotels.at/hotel-bellevue

For further information please take a look at:
http://so-logic.net/en/after_work/hotel

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Catering

Lunch

For the lunch there will be finger food and sweet cakes.

Dinner

A buffet with a rich variation of dishes will be arranged

Drinks

Nesspresso coffee, tea and soft drinks are being served during the hole presentation and the breaks. During dinner wine and draught beer will also be offered.

Provider

Daniela Cakes
www.danielasantos.com

Daniela Santos is a successful cake designer, demonstrator of cake decoration and sugar craft specializing in cake sculpture and modeling.

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Exhibition

Rosangela Scheithauer is an Artist born in Mogi Mirim (Sao Paulo), Brazil. She has been living and working in Vienna (Austria) for the past 23 years. Rosangela studied Arts from 1986 to 1989 at the Brera Academy of Arts in Milan, Italy, under the tutorship of the renowned Professor Carlo Righi. Her paintings transmit all the sensibility which is expressed pictorically throughout her work. With her brushes she invites the admirer to a daydream of culture throughout her country. Lately she has devoted herself to abstract paintings because they give her freedom and a sense of magic too.

www.rosangelascheithauer.at

Sightseeing in Vienna

Enjoy your time in Vienna
There is much to see: From gothic St. Stephen's Cathedral to the Imperial Palace, from the magnificent baroque palace Schönbrunn to the Museum of Fine Arts.
Record-breaking: In Vienna, there are over 27 castles and more than 150 palaces.

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Contact

for further information
please visit:

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or please contact:

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Getting to the event location:

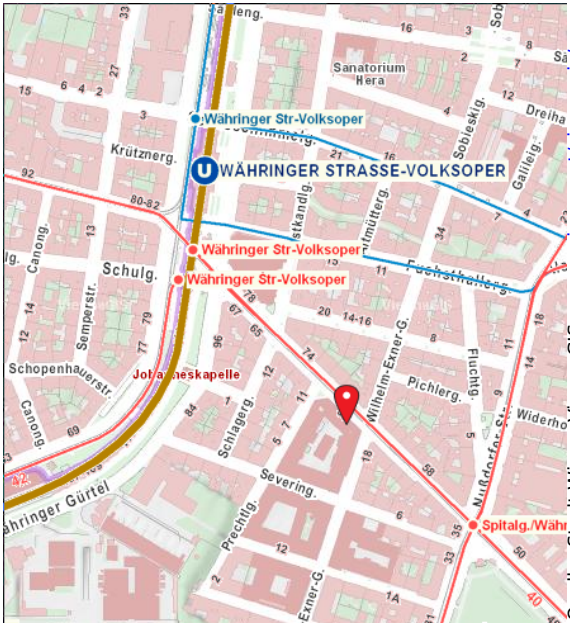
WUK
Werkstätten- und Kulturhaus

Währinger Straße 59
A-1090 Vienna
www.wuk.at

Arriving at railway station "Westbahnhof"
take the underground line U6 direction Floridsdorf exit "Währinger Straße"

Arriving at the airport
you will take the Vienna Airport Lines (Bus) to "Westbahnhof" and continue as written above

Arriving at railway station "Südbahnhof"
take the "Schnellbahn" to "Wien Meidling" then the underground line U6 direction Floridsdorf exit "Währinger Straße"



Quelle: Stadt Wien - ViennaGIS - www.wien.gv.at/viennagis/

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